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PATENT

Our Reference: ENL-197-A

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Jan Nigel Harvey  
Serial Number: 09/010,256  
Filing Date: January 21, 1998  
Examiner/Art Group Unit: Y. Encarnacion/2751  
Title: MICROPROCESSOR CACHE  
CONSISTENCY

MAR 06 2000  
PATENT & TRADEMARK OFFICE

AMENDMENT

Assistant Commissioner of Patents  
Washington, D.C. 20231

Sir:

If any charges or fees must be paid in connection with the following communication, they may be paid out of our Deposit Account No. 25-0115.

The Office Action dated October 26, 1998 has been received and carefully reviewed. Please amend the above-identified patent application as indicated below.

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TC 2700 MAIL ROOM

In the claims:

Please cancel claims 1-8.

Please add the following new claims:

- 1 8. (New). A method of managing memory in a  
2 system wherein the system comprises:  
3 at least two processors and a system memory,  
4 each processor having a cache memory; and  
5 wherein the system memory is divided into pages  
6 each of which initially has a "free" status and is  
7 subdivided into unallocated blocks;  
8 wherein the method comprises:  
9 if a first block of memory is required for  
10 storage of data local to a specific processor then:

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